IN THE CLAIMS

Please amend claims 1, 4 and 13 as follows below.

1. (Currently amended) A method of forming at least a portion of a dual bit memory core array upon a semiconductor substrate, the method comprising:

forming a charge trapping dielectric layer over the substrate;

forming a hardmask over the charge trapping dielectric layer;

patterning the hardmask to form a plurality of hardmask features having a first spacing therebetween;

forming a spacer material over the patterned hardmask;

patterning the spacer material to form spacers adjacent the hardmask features and defining a second spacing between the hardmask features that is less than the first spacing;

performing a bitline implant through the charge trapping dielectric to establish buried bitlines within the substrate having a width corresponding to the second spacing;

removing the entire patterned hardmask and all the spacers associated with the patterned hardmask;

forming a wordline material over the charge trapping dielectric layer; and

patterning the wordline material to form wordlines that overlie the bitlines.

2. (Original) The method of claim 1, wherein the substrate is p-type and the bitline implant is performed with an n-type dopant, and wherein the spacers inhibit the dopant from being implanted there-under, the spacers thus serving to establish bitlines that are narrower than the first spacing.

3. (Original) The method of claim 2, wherein the bitline implant dopant includes Arsenic.

4. (Currently amended) The method of claim [[5]] 3, wherein the bitline

implant is performed at a concentration of between about 5E14 and 2E15 atoms/cm3.

5. (Original) The method of claim 3, wherein the bitline implant is performed at an energy level of between about 40 to 70KeV.

6. (Original) The method of claim 1, wherein forming a charge trapping dielectric layer comprises:

forming a first insulating layer over the semiconductor substrate;

forming a charge trapping layer over the first insulating layer; and

forming a second insulating layer over the charge trapping layer.

7. (Original) The method of claim 6, wherein the first and second insulating layers comprise silicon dioxide.

8. (Original) The method of claim 6, wherein the charge-trapping layer comprises silicon nitride.

9. (Original) The method of claim 6, wherein the first insulating layer is formed to a thickness of about 70 Angstroms or less.

10. (Original) The method of claim 6, wherein the charge trapping layer is formed to a thickness of between about 60 to 80 Angstroms.

11. (Original) The method of claim 6, wherein the second insulating layer is formed to a thickness of about 100 Angstroms or less.

12. (Original) The method of claim 6, further comprising:

removing the second insulating layer; and

re-applying the second insulating layer to a thickness of about 100 Angstroms or

less.

13. (Currently amended) The method of claim 12, wherein the ~~sacrificial oxide~~ removed second insulating layer layer is initially formed to a thickness of between about 100 to 200 Angstroms.

14. (Original) The method of claim 1, wherein at least one of the hardmask and spacers are formed of nitride or poly-based material(s).

15. (Original) The method of claim 2, wherein the implanted bitlines have a width of between about 40 to 100 nano-meters or less.

16. (Original) The method of claim 1, wherein the wordlines are oriented at substantially right angles relative to the buried bitlines.

17. (Original) The method of claim 1, comprising:

performing a threshold adjustment implant into the semiconductor substrate prior to forming the charge trapping dielectric layer.

18. (Original) The method of claim 17, wherein the substrate is doped with a p-type dopant and the threshold adjustment implant includes at least one of a greater concentration of and a higher energy implant of the same or different p-type dopant.

19. (Original) The method of claim 18, wherein the threshold adjustment implant includes Boron.

20. (Original) The method of claim 1, wherein the substrate comprises silicon.

21. (Original) A method of forming at least a portion of a dual bit memory core

array upon a semiconductor substrate, the method comprising:

forming at least a portion of a charge trapping dielectric layer over the substrate;

forming a layer of sacrificial material over the portion of the charge trapping dielectric layer;

forming a hardmask over the sacrificial layer;

patterning the hardmask to form a plurality of hardmask features having a first spacing therebetween;

forming a spacer material over the patterned hardmask;

patterning the spacer material to form spacers adjacent the hardmask features and defining a second spacing between the hardmask features that is less than the first spacing;

performing a bitline implant through the portion of the charge trapping dielectric layer to establish buried bitlines within the substrate having a width corresponding to the second spacing;

removing the patterned hardmask and spacers; and

forming a remaining portion of the charge trapping layer over the portion of the charge trapping dielectric layer.

22. (Original) The method of claim 21, wherein forming at least a portion of a charge trapping dielectric layer comprises:

forming a first insulating layer over the semiconductor substrate; and

forming a charge trapping layer over the first insulating layer.

23. (Original) The method of claim 22, wherein forming a layer of sacrificial material comprises:

forming a second insulating layer over the charge trapping layer.

24. (Original) The method of claim 23, wherein the first and second insulating layers comprise silicon dioxide.

25. (Original) The method of claim 22, wherein the charge-trapping layer comprises silicon nitride.

26. (Original) The method of claim 22, wherein the first insulating layer is formed to a thickness of about 70 Angstroms or less.

27. (Original) The method of claim 22, wherein the charge trapping layer is formed to a thickness of between about 60 to 80 Angstroms.

28. (Original) The method of claim 21, wherein the remaining portion of the charge trapping layer is formed to a thickness of about 100 Angstroms or less.

29. (Original) The method of claim 21, wherein the layer of sacrificial material is formed to a thickness of between about 100 to 200 Angstroms.

30. (Original) The method of claim 21, wherein the implanted bitlines have a width of between about 40 to 100 nano-meters or less.

31. (Original) The method of claim 21, further comprising:
forming a wordline material over the charge trapping dielectric layer; and
patterning the wordline material to form wordlines that overlie the bitlines.